CLAIMS

- 1 1. A method for forming a trimmed gate in a transistor comprising the steps of:
- 2 forming a polysilicon portion of a gate conductor on a substrate having a
- 3 semiconductor portion; and
- 4 trimming the polysilicon portion by a selective film growth method.
- 1 2. The method of claim 1, wherein the selective film growth method comprises
- 2 selective surface nitridation.
- 1 3. The method of claim 1, wherein the selective film growth method comprises
- 2 selective surface oxidation.
- 1 4. The method of claim 1, wherein the step of trimming the polysilicon portion
- 2 further comprises selectively compensating n-channel and p-channel devices.
- 1 5. The method of claim 1, additionally comprising the step of at least partially
- 2 removing the trimming film.
- 1 6. The method of claim 1, wherein the trimming film is anisotropically etched,
- 2 forming gate conductor spacers.
- 1 7. The method of claim 1, wherein the trimming film is silicon-rich and the method
- 2 further comprises the step of forming additional nitride or oxide layers on the trimming
- 3 film.

- 1 8. The method of claim 2, wherein the step of trimming the gate conductor by
- 2 selective surface nitridation comprises exposing structures formed on the semiconductor
- 3 portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 200-700
- 4 mJ/cm² in the presence of ammonia at a pressure of 10-1500 torr.
- 1 9. The method of claim 8, wherein the step of trimming the gate conductor by
- 2 selective surface nitridation comprises exposing structures formed on the semiconductor
- 3 portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of
- 4 400-500 mJ/cm² in the presence of ammonia at a pressure of about 300-500 torr.
- 1 10. The method of claim 9, wherein ammonia is supplied at about 100 ccm/min.
- 1 11. The method of claim 3, wherein the step of trimming the gate conductor by
- 2 selective surface oxidation comprises exposing structures formed on the semiconductor
- portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 100-600
- 4 mJ/cm² in the presence of oxygen at a pressure of 1-760 torr.
- 1 12. The method of claim 11, wherein the step of trimming the gate conductor by
- 2 selective surface oxidation comprises exposing structures formed on the semiconductor
- 3 portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of
- 4 200-400 mJ/cm² in the presence of oxygen at a pressure of about 100-300 torr.
- 1 13. The method of claim 12, wherein oxygen is supplied at about 100 ccm/min.

- 1 14. A method for forming selectively compensated semiconductor devices comprising
- 2 the steps of:
- forming a plurality of polysilicon portions of gate conductors on a substrate
- 4 having a semiconductor portion;
- 5 masking at least one polysilicon portion intended for a n-channel device;
- trimming at least one unmasked polysilicon portion intended for a p-channel
- 7 device by a selective film growth method, wherein the extent of trimming is selected to
- 8 accomplish device compensation of the p-channel and n-channel devices.
- 1 15. The method of claim 14, wherein the selective film growth method comprises
- 2 selective surface nitridation.
- 1 16. The method of claim 14, wherein the selective film growth method comprises
- 2 selective surface oxidation.
- 1 17. The method of claim 15, wherein the step of trimming the gate conductor by
- 2 selective surface nitridation comprises exposing structures formed on the semiconductor
- 3 portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of
- 4 400-500 mJ/cm² in the presence of ammonia at a pressure of about 300-500 torr.
- 1 18. The method of claim 16, wherein the step of trimming the gate conductor by
- 2 selective surface oxidation comprises exposing structures formed on the semiconductor
- 3 portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of
- 4 200-400 mJ/cm² in the presence of oxygen at a pressure of about 100-300 torr.

- 1 19. A transistor comprising a trimmed polysilicon portion of a gate conductor,
- 2 wherein the trimming occurred by a selective film growth method.
- 1 20. The transistor of claim 19, wherein n-channel and p-channel devices were
- 2 selectively compensated by the trimming.
- 1 21. The transistor of claim 19, wherein a sufficient portion of the trimming film is
- 2 removed by anisotropic etching to provide gate conductor spacers.
- 1 22. The transistor of claim 19, wherein the trimming film is silicon-rich, allowing
- 2 additional nitride or oxide layers to be formed.
